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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,643	10/29/2003	Tomohiro Takamatsu	032057	5393

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EXAMINER	
ERDEM, FAZLI	
ART UNIT	**PAPER NUMBER**
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/695,643	TAKAMATSU ET AL.	
	Examiner	Art Unit	
	FAZLI ERDEM	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-10 and 12-33* is/are pending in the application.

4a) Of the above claim(s) *17-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-10,12-16 and 33* is/are rejected.

7)☐ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/03/2008 has been entered.

Allowable Subject Matter

2. The indicated allowability of claims 9, 10, and 12-16 is withdrawn in view of the newly discovered reference(s) to Ri et al. Rejections based on the newly cited reference(s) follow.

3. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

4. Applicant's arguments with respect to claims 1-5 and 8-16 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 9, 10, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suenaga et al. (6,239,457) in view of Ri et al. (JP 2001085624). In the examiner's opinion, this/these claim(s) would have been obvious according to one of the rationales expressed in the *Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103 in View of the Supreme Court Decision in KSR International Co. v. Teleflex Inc.*, as published at 72 Federal Register 57526 et seq.[1] (10/10/2007).

The Guidelines explain that an invention that would have been obvious to a person of ordinary skill at the time of the invention is not patentable. The Guidelines point out that, as reiterated by the Supreme Court in KSR, the framework for the objective analysis for determining obviousness under 35 U.S.C. 103 is stated in *Graham v. John Deere Co.* Obviousness is a question of law based on underlying factual inquiries. The factual inquiries enunciated by the Court are as follows:

> (1) Determining the scope and content of the prior art;
> (2) Ascertaining the differences between the claimed invention and the prior art, and
> (3) Resolving the level of ordinary skill in the pertinent art.

Examining this last factor first, it is noted that any obviousness rejection should include, either explicitly or implicitly in view of the prior art applied, an indication of the level of ordinary skill. This is an essential finding because (as the Guidelines point out) a finding as to the level of ordinary skill may be used as a partial basis for a resolution of the issue of obviousness. The person of ordinary skill in the art is a hypothetical person

[1] Available at http://www.uspto.gov/web/offices/com/sol/notices/72fr57526.pdf

who is presumed to have known the relevant art at the time of the invention. Factors that may be considered in determining the level of ordinary skill in the art include:

(1) "Type of problems encountered in the art;"
(2) "prior art solutions to those problems;"
(3) "rapidity with which innovations are made;"
(4) "sophistication of the technology;" and
(5) "educational level of active workers in the field."

In a given case, every factor may not be present, and one or more factors may predominate.

In the present case, Applicant has presented claims to a device classified in Class 257 (Semiconductor Devices). The types of problems encountered in Class 257 typically are highly complex, involving questions of electrodynamics, thermodynamics, crystallography, and quantum mechanics. Prior art solutions to the problems presented in this field demonstrate thinking of the highest order. Many prior art solutions in this field have won Nobel prizes. Past Nobel prizewinners for Class 257 innovations include John Bardeen, William Schockley, Jack Kilby, Leo Esaki, Nick Basow, Zhores Alferov, Pierre-Gilles de Gennes, and probably a half dozen more this writer has forgotten. Innovations in Class 257 are made with extremely high rapidity (see, e.g. "Moore's Law"). Technology used to make and practice inventions in this field are highly sophisticated. Some "fabs" (as those of skill in the art call the factories for making these devices) now cost in excess of one billion dollars each, and perform literally hundreds of billions of operations per hour. Finally, the educational level of active workers in this field is extremely high – Ph.D.s are common, and a bachelor's degree in engineering is the absolute minimum educational level of workers in this field.

In short, the level of ordinary skill in this field is extremely high. In KSR, the Supreme Court cautioned, "A person of ordinary skill is also a person of ordinary creativity." *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1742, 82 USPQ2d 1385, 1397 (2007). Had the Court taken a look at the people who have practiced the semiconductor art in the past and the variety of extraordinarily valuable (from lifestyle-changing, such as high-speed communications and computing, to handy devices such as IPods and cellphones) and difficult solutions to challenging problems those people have accomplished, the Examiner is convinced the Court would have said that in the semiconductor art the person of ordinary skill is a person of extraordinary creativity.

Next, we consider the first and second factual findings required by *Graham*. The scope and content of the prior art includes, n Figs. 1A, 6, 7A, 7B, 8A-8D and 10, Suenaga et al. disclose a semiconductor memory device comprising: an insulating film 102 in Fig 10, formed over a semiconductor substrate 98; an adhesive layer 81 formed on the insulating film; a capacitor lower electrode 11 formed on the adhesive layer, a ferroelectric layer 104 formed on the capacitor lower electrode, and having an ABO_3 perovskite structure (A=any one of Bi, Pb, Ba, Sr, Ca, Na, K, and a rare earth element, B=any one of Ti, Zr, Nb, Ta, W, Mn, Fe, Co, and Cr) as disclosed in column 2, lines 34-55 and an upper capacitor electrode 105 formed on the ferroelectric layer.

Regarding Claim 10, it is disclosed in Suenaga et al. that ferroelectric layer has preferred the orientation is perpendicular to substrate pane hence 0 degrees inclination from perpendicular direction which would satisfy 3.5 degrees or LESS claim language), a ferroelectric layer 104 formed on the capacitor lower electrode, and having an ABO3

perovskite structure (A=any one of Bi, Pb, Ba, Sr, Ca, Na, K, and a rare earth element, B=any one of Ti, Zr, Nb, Ta, W, Mn, Fe, Co, and Cr) as disclosed in column 2, lines 34-55

Regarding Claim 12, in Suenaga et al., lower electrode 11 is Pt or Ir as disclosed column 2 lines 22-33

Regarding Claim 13, Fig 3 of Suenaga et al. disclose PZT based ferroelectric layer 104.

The difference between the prior art semiconductor memory device disclosed by Suenaga et al. and the claimed device is that, where the claim requires an adhesive layer having a surface roughness of 0.79 nm or less, Suenaga et al.'s semiconductor memory device includes an adhesive layer having a surface roughness of 2-3 nm.

However, Ri et al. discloses an iridium electrode 4 (said electrode being identical, as far as electrodes go, to Suenaga et al.'s electrode) attached via adhesive layer 7 to an underlying insulator. Adhesive layer 7 has an average surface roughness of 0.1-0.5 nm. Note figures 1-4 of Ri et al. and the accompanying abstract/partial translation. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claims 9, 10 and 12-16 by substituting the adhesive layer with a 0.1-0.5 nm surface roughness taught by Ri et al. for Suenaga et al.'s adhesive layer having a surface roughness of 2-3 nm?

To reject a claim based on the basis of the rationale expressed in section IIIB of the Examination Guidelines, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

> (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
>
> (2) a finding that the substituted components and their functions were known in the art;
>
> (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
>
> (4) whatever additional findings based on the *Graham* factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Suenaga et al. discloses a device (semiconductor memory device) that differed from the claimed device only by the substitution of some components (an adhesive layer having a surface roughness of 0.79 nm or less) for other components (an adhesive layer having a surface roughness of 2-3 nm). Ri et al. discloses that the substituted components and their functions were known in the art. Further, Ri et al. discloses that those of skill in the art were familiar with a method of combining an adhesive layer with a 0.1-0.5 nm surface roughness with an Iridium electrode similar to the Iridium electrode of Suenaga et al.'s semiconductor memory device. From the similarities between Ri et al.'s Iridium electrode and the Iridium electrode of Suenaga et al.'s semiconductor memory device, one of skill in the art would have been able to conclude that an adhesive layer with a 0.1-0.5 nm surface roughness could have substituted for the adhesive layer having a surface roughness of 2-3 nm of Suenaga et al.'s semiconductor memory device. One of skill in the art would have had reason to predict (based on its functioning in combination with Ri et al.'s Iridium electrode) that the adhesive layer with a 0.1-0.5 nm surface roughness would have

continued functioning much as it did in combination with Ri et al.'s Iridium electrode, and that after the substitution, Suenaga et al.'s semiconductor memory device would continue functioning in the manner disclosed by Suenaga et al.. It would therefore have been obvious to a person having skill in the art to modify Suenaga et al.'s semiconductor memory device by substituting the adhesive layer with a 0.1-0.5 nm surface roughness taught by Ri et al. for Suenaga et al.'s adhesive layer having a surface roughness of 2-3 nm.

7. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suenaga et al. (6,239,457) in view of Ri et al. (JP 2001085624), as applied to claim 9, above, and further in view of Asano (6,407,422)

Suenaga et al. and Ri et al. suggest a semiconductor memory device having all the limitations of claims 14, 15, and 16 except a hole formed in the insulating film and the adhesive layer under the lower electrode; a conductive plug formed in the hole and connected to the lower electrode; and an oxygen barrier metal layer constituting a part of the lower electrode formed between the conductive plug and the lower electrode.

However, Asano et al. disclose an oxygen diffusion blocking semiconductor capacitor where in Fig. 5, oxygen barrier layer 53/52 are disclosed between the plug, which extends in insulating layer 13 and adhesion layer 51, and the lower electrode 32.

Regarding Claim 14, in Fig. 1A of Asano et al, hole 14 is formed in the insulating film 113 and the adhesive layer 51 under the lower electrode; and a conductive plug 15 formed in the hole and connected to the lower electrode 32

Regarding Claim 15, in Fig. 1A of Asano et al. oxygen barrier metal layer 52/53 is formed between the conductive plug 15 and the lower electrode 32.

Regarding Claim 16, Asano et al.'s oxygen barrier metal layer 52 constitutes a part of the lower electrode 32.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the oxygen barrier as taught Asano et al. in order to have a increased stability and diffusion characteristics between the lower electrode and the ferroelectric layer and in order to even the interface between the lower electrode and the adhesive layer.

8. Claims 1-5, 7, 8, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suenaga et al. (6,239,457) in view of Ri et al. (JP 2001085624).and Vente et al. (Journal of Solid State Chemistry, as submitted by the applicant on 12/7/2006).

With regard to claims 1-5, 7, 8, and 33 we begin by considering the first and second factual findings (the third finding concerning the level of skill in the art, is the same as before. The level of skill in the semiconductor art is a level of creativity, scientific thinking, and applied problem-solving unprecedented in the history of Man) required by *Graham*. The scope and content of the prior art includes, in Figs. 1A, 6, 7A, 7B, 8A-8D and 10, Suenaga et al. disclose a semiconductor memory device comprising: an insulating film 102 in Fig 10, formed over a semiconductor substrate 98; an adhesive layer 81 formed on the insulating film; a capacitor lower electrode 11 formed on the adhesive layer, a ferroelectric layer 104 formed on the capacitor lower electrode, and

having an ABO_3 perovskite structure (A=any one of Bi, Pb, Ba, Sr, Ca, Na, K, and a rare earth element, B=any one of Ti, Zr, Nb, Ta, W, Mn, Fe, Co, and Cr) as disclosed in column 2, lines 34-55 and an upper capacitor electrode 105 formed on the ferroelectric layer.

Regarding Claims 2 and 33, it is disclosed in Suenaga et al. that ferroelectric layer has an orientation perpendicular to substrate plane. This results in 0 degrees inclination from perpendicular direction which would satisfy the 2.3 degrees or LESS limitation of claim 33 as well as the 3.5 degrees or LESS limitation of claim 2), a ferroelectric layer 104 formed on the capacitor lower electrode, and having an ABO3 perovskite structure (A=any one of Bi, Pb, Ba, Sr, Ca, Na, K, and a rare earth element, B=any one of Ti, Zr, Nb, Ta, W, Mn, Fe, Co, and Cr) as disclosed in column 2, lines 34-55

Regarding Claim 3, Fig 3 of Suenaga et al. disclose PZT based ferroelectric layer 104.

Regarding Claim 4, it is disclosed in Suenaga et al. that ferroelectric layer has preferred the orientation is perpendicular to substrate pane hence 0 degrees inclination from perpendicular direction which would satisfy 2.3 degrees or LESS claim language), a ferroelectric layer 104 formed on the capacitor lower electrode, and having an ABO3 perovskite structure (A=any one of Bi, Pb, Ba, Sr, Ca, Na, K, and a rare earth element, B=any one of Ti, Zr, Nb, Ta, W, Mn, Fe, Co, and Cr) as disclosed in column 2, lines 34-55

Regarding Claim 5, in Suenaga et al., lower electrode 11 is Pt or Ir as disclosed column 2 lines 22-33

Regarding Claim 8, upper electrode of Suenaga et al. is Pt or Ir as disclosed column 2 lines 22-33

One difference between the prior art semiconductor memory device disclosed by Suenaga et al. and the claimed device is that, where the claim requires an adhesive layer having a surface roughness of 0.79 nm or less, Suenaga et al.'s semiconductor memory device includes an adhesive layer having a surface roughness of 2-3 nm.

However, Ri et al. discloses an iridium electrode 4 (said electrode being identical, as far as electrodes go, to Suenaga et al.'s electrode) attached via adhesive layer 7 to an underlying insulator. Adhesive layer 7 has an average surface roughness of 0.1-0.5 nm. Note figures 1-4 of Ri et al. and the accompanying abstract/partial translation.

Another difference between the prior art semiconductor memory device disclosed by Suenaga et al. and the claimed device is that, where the claim requires a ferroelectric layer having an ABO_3 perovskite structure that contains Ir in at least one of an A site and a B site (A=any one of Bi, Pb, Ba, Sr, Ca, Na, K, and a rare earth element, B=any one of Ti, Zr, Nb, Ta, W, Mn, Fe, Co, and Cr), Suenaga et al.'s semiconductor memory device includes a ferroelectric layer having an ABO_3 perovskite structure where A=Pb, B=(Zr_{1-x}, Ti_x)

However, Vente et al. disclose a perovskite $BaIrCoO_3$ that includes Ba in A site, Co in B site and Ir in at least one of A or B site as shown in pages 361-363.

The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claims 9, 10 and 12-16 by substituting the adhesive layer with a 0.1-0.5 nm surface roughness taught by Ri et al. for Suenaga et al.'s adhesive layer having a surface roughness of 2-3 nm, and by substituting the $BaIrCoO_3$ taught by Vente et al. for Suenaga et al.'s ABO_3 perovskite structure?

To reject a claim based on the basis of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

> (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
>
> (2) a finding that the substituted components and their functions were known in the art;
>
> (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
>
> (4) whatever additional findings based on the *Graham* factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Suenaga et al. discloses a device (semiconductor memory device) that differed from the claimed device only by the substitution of some components (an adhesive layer having a surface roughness of 0.79 nm or less) for other components (an adhesive layer having a surface roughness of 2-3 nm), and by the substitution of a second set of components (a ferroelectric layer having an ABO_3 perovskite structure that contains Ir in at least one of an A site and a B site (A=any one of Bi, Pb, Ba, Sr, Ca, Na, K, and a rare earth element, B=any one of Ti, Zr, Nb, Ta, W, Mn, Fe, Co, and Cr)) for other components (an ABO_3 perovskite structure).

Ri et al. discloses that the substituted components and their functions were known in the art. Further, Ri et al. discloses that those of skill in the art were familiar with a method of combining an adhesive layer with a 0.1-0.5 nm surface roughness with an Iridium electrode similar to the Iridium electrode of Suenaga et al.'s semiconductor memory device. From the similarities between Ri et al.'s Iridium electrode and the Iridium electrode of Suenaga et al.'s semiconductor memory device, one of skill in the art would have been able to conclude that an adhesive layer with a 0.1-0.5 nm surface roughness could have substituted for the adhesive layer having a surface roughness of 2-3 nm in contact with the iridium electrode of Suenaga et al.'s semiconductor memory device. One of skill in the art would have had reason to predict (based on its functioning in combination with Ri et al.'s Iridium electrode) that the adhesive layer with a 0.1-0.5 nm surface roughness would have continued functioning much as it did in combination with Ri et al.'s Iridium electrode, and that after the substitution, Suenaga et al.'s semiconductor memory device would continue functioning in the manner disclosed by Suenaga et al.. It would therefore have been obvious to a person having skill in the art to modify Suenaga et al.'s semiconductor memory device by substituting the adhesive layer with a 0.1-0.5 nm surface roughness taught by Ri et al. for Suenaga et al.'s adhesive layer having a surface roughness of 2-3 nm.

Further, Vente et al. discloses that the Ir-ABO_3 substituted components and their functions were known in the art. Vente et al. discloses that those of skill in the art were familiar with a method of combining iridium with an ABO_3 perovskite structure, a device very similar to Suenaga et al.'s ABO_3 perovskite structure. From the similarities between